Results for "(wang m.<in>au) and fpga" e-mail
Your search matched **9** of **1340257** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

(wang m.<in>au) and fpga Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

| | |
|---|---|
| IEEE JNL | IEEE Journal or Magazine |
| IEE JNL | IEE Journal or Magazine |
| IEEE CNF | IEEE Conference Proceeding |
| IEE CNF | IEE Conference Proceeding |
| IEEE STD | IEEE Standard |

view selected items Select All Deselect All

1. **A general-purpose VME module**
Guo, Y.N.; Gao, Z.W.; Chang, M.C.; Li, H.H.; Wang, M.Z.;
Nuclear Science, IEEE Transactions on
Volume 50, Issue 5, Part 3, Oct. 2003 Page(s):1752 - 1755
Digital Object Identifier 10.1109/TNS.2003.818272
AbstractPlus | References | Full Text: PDF(483 KB) IEEE JNL
Rights and Permissions

2. **The application of tiny triplet finder (TTF) in btev pixel trigger**
Wu, J.; Wang, M.; Gottschalk, E.; Shi, Z.;
Real Time Conference, 2005. 14th IEEE-NPSS
June 4-10, 2005 Page(s):108 - 112
AbstractPlus | Full Text: PDF(343 KB) IEEE CNF
Rights and Permissions

3. **A commodity solution based high data rate asynchronous trigger system collider experiments**
Wang, M.; Jin Yuan Wu;
Real Time Conference, 2005. 14th IEEE-NPSS
June 4-10, 2005 Page(s):228 - 232
AbstractPlus | Full Text: PDF(244 KB) IEEE CNF
Rights and Permissions

4. **Integrated upstream parasitic event building architecture for BTeV level 1 system**
Jinyuan Wu; Wang, M.; Gottschalk, E.; Christian, D.; Li, X.; Shi, Z.; Pavlicek, V
Real Time Conference, 2005. 14th IEEE-NPSS
June 4-10, 2005 Page(s):607 - 611
AbstractPlus | Full Text: PDF(396 KB) IEEE CNF
Rights and Permissions

5. **Configurable area-IO memory for system-in-a-package (SiP)**
Wang, M.; Suzuki, K.; Dai, W.; Sakai, A.; Watanabe, K.;
Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27t
18-20 Sept. 2001 Page(s):385 - 388
AbstractPlus | Full Text: PDF(848 KB) IEEE CNF
Rights and Permissions

Author Search

**OPTION 1**
Quick Find an Author:
Enter a name to locate articles written by that author.

Chiu V

Example: Enter Lockett S to obtain a list of authors with the last name Lockett and the first initial S.

**OPTION 2**
Browse alphabetically

Select a letter from the list.

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

**No Authors found beginning with letter: Chiu V**

Search Session History

**Tue, 18 Apr 2006, 10:31:31 AM EST**

Edit an existing query or compose a new query in the Search Query Display.

**Select a search number (#) to:**

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Search Query Display

Recent Search Queries

| | |
|---|---|
| #1 | ((an efficient logic simulation system)<in>metadata) |
| #2 | (butts m.<in>au) |
| #3 | (butts m.<in>au) |
| #4 | (butts m.<in>au) |
| #5 | ((an efficient logic simulation system)<in>metadata) |
| #6 | (BORG: a reconfigurable prtotyping board using field-programmabie<iN>metadata) |
| #7 | (schlag m.<in>au) |
| #8 | (multi-FPGA emulation<IN>metadata) |
| #9 | (an fpga-based reconfigurable system<IN>metadata) |
| #10 | (an fpga-based reconfigurable system<IN>metadata) |

# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 2 | "6507920".pn. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 13:12 |
| L2 | 901 | serial same bus same emulat$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 13:12 |
| L3 | 422 | serial adj bus$3 same emulat$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 13:13 |
| L4 | 143 | serial adj bus$3 near6 (emulat$3 or simulat$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 13:13 |
| L5 | 97 | L4 and @ad<"20020801" | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:26 |
| L6 | 0 | simulat$3 same transportation same particle same distribution and ray and voxel | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:27 |
| L7 | 1 | simulat$3 same particle same distribution and ray and voxel and transporta$4 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:28 |
| L8 | 6 | simulat$3 same particle same distribution and ray and voxel | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:38 |
| L9 | 78 | emulat$4 same FPGA same network | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:57 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| L10 | 65 | L9 and @ad<"20030601" | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:57 |
| L11 | 122 | emulat$4 same FPGA and network adj interface | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:57 |
| L12 | 105 | L11 and @ad<"20030601" | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:57 |
| L13 | 66 | L12 and behavior | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/18 14:58 |

Google Scholar BETA multi-FPGA network interface Search Advanced Scholar Search Scholar Preferences Scholar Help

**Scholar** Results **1 - 10** of about **232** for **multi-FPGA network interface**. (**0.10** seconds)

Baring it all to Software: The Raw Machine - group of 11 »
E Waingold, M Taylor, V Sarkar, W Lee, V Lee, J ... - IEEE Computer, 1997 - aar.cs.ucdavis.edu
... The onerous compile times of our **multi-FPGA** based Raw prototype computer (see Section 6 ... The processor/**network interface** is shared between the two networks. ...
Cited by 287 - View as HTML - Web Search - BL Direct

[PS] The Transmogrifier: The University of Toronto Field-Programmable System
D Galloway, D Karchmer, P Chow, D Lewis, J Rose - Second Canadian Workshop on Field-Programmable Devices, ..., 1994 - eecg.toronto.edu
... **Interface** Board ... 4. TM-1 Interconnection **Network** In typical **multi-FPGA** boards, eg [Gokhale91], the wires that connect the FPGAs together are usually hard-wired ...
Cited by 22 - View as HTML - Web Search

Logic Partition Orderings for **Multi-FPGA** Systems - group of 10 »
S Hauck, G Borriello - FPGA, 1995 - doi.ieeecomputersociety.org
... Logic Partition Orderings for **Multi-FPGA** Systems ... This allows **multi-FPGA** partitioners to harness standard partitioning techniques. ...
Cited by 15 - Web Search

A hardware implementation of a signaling protocol - group of 5 »
H Wang, M Veeraraghavan, R Karri - Proc. of Opticomm 2002 - ece.virginia.edu
... is that an out-of-band IP **network** will be ... timeslot pair and the outgoing **interface**/timeslot pair ... We used the WILDFORCE TM **multi-FPGA** reconfigurable computing ...
Cited by 14 - View as HTML - Web Search

Scalable Pattern Matching for High Speed Networks - group of 6 »
CR Clark, DE Schimmel - Proc. IEEE Symposium on Field-Programmable Custom Computing ..., 2004 - ieeexplore.ieee.org
... devices such as routers, switches, and **network interface** cards. At the upper end of the application spectrum, we envision larger, **multi- FPGA** systems operating ...
Cited by 8 - Web Search

Hardware spiking neural **network** with run-time reconfigurable connectivity in an autonomous robot - group of 8 »
D Roggen, S Hofmann, Y Thoma, D Floreano - Proc. 2003 NASA/DOD Conference on Evolvable Hardware, July, 2003 - doi.ieeecomputersociety.org
... I/O for the Khepera bus or user I/O • Stackable modules (**multi-FPGA** system sharing a ... UART and I/O) 2121 17.9ns • **Network interface** 163 7.83ns • Net. ...
Cited by 6 - Web Search

[PS] Interconnect Synthesis for Reconfigurable **Multi-FPGA** Architectures - group of 7 »
V Srinivasan, S Radhakrishnan, R Vemuri, J Walrath - bdd (Binary Decision Diagram) - ececs.uc.edu
... pipelined routing algorithm for **multi-FPGA** systems. ... through an api (Application Procedural **Interface**). ... that makes the interconnection **network** implement the ...
Cited by 6 - View as HTML - Web Search - BL Direct

Implementation of BEE: a real-time large-scale hardware emulation engine - group of 7 »
C Chang, K Kuusilinna, B Richards, RW Brodersen - FPGA, 2003 - portal.acm.org
... Figure 3: Various **multi-FPGA** interconnect topologies In light of the above two

# Routing on field-programmable switch matrices

**Source** **IEEE Transactions on Very Large Scale Integration (VLSI) Systems** archive
Volume 11 , Issue 2 (April 2003) table of contents
Pages: 283 - 287
Year of Publication: 2003
ISSN:1063-8210

**Authors** Abdel Ejnioui School of Electrical Engineering and Computer Science, University of Central Florida, Orlando, FL
N. Ranganathan Department of Computer Science and Engineering, University of South Florida, Tarapa, FL

**Publisher** IEEE Educational Activities Department Piscataway, NJ, USA

Author Search

OPTION 1
Quick Find an Author:
Enter a name to locate articles written by that author.

Ngui N

Example: Enter Lockett S to obtain a list of authors with the last name Lockett and the first initial S.

OPTION 2
Browse alphabetically

Select a letter from the list.

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

**No Authors found beginning with letter: Ngui N**